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What is claimed is:

1. A computerized method of creating a layout for a circuit design, the method comprising:

receiving a circuit design;

receiving at least one layout rule based on a reliability verification constraint for the circuit design; and

generating a layout for the circuit design through computer automated operations wherein the layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

2. The computerized method of claim 1, wherein the reliability verification constraint arises from electromigration.

3. The computerized method of claim 1, wherein the reliability verification constraint arises from self-heat.

4. The computerized method of claim 1, wherein the at least one layout rule defines a maximum current for a given wire width.

5. The computerized method of claim 1, wherein the circuit design is a microprocessor circuit design.

6. The computerized method of claim 1, wherein the layout is a two-dimensional layout comprising a plurality of overlapping rows.

7. A computer automated placement method comprising:

placing a plurality of components of an integrated circuit design in a layout for the integrated circuit design;

analyzing the layout for reliability verification considerations;

rearranging the plurality of components to improve the reliability verification considerations; and

repeating the analyzing and the rearranging to further improve the reliability verification considerations.

8. The computer automated placement method of claim 7, wherein analyzing the layout for reliability verification considerations includes analyzing for electromigration considerations.

9. The computer automated placement method of claim 7, wherein analyzing the layout for reliability verification considerations includes analyzing for self heat considerations.

10. The computer automated placement method of claim 7, further comprising analyzing the layout for other considerations selected from the group consisting of: layout density constraints, aspect ratio constraints, and routing complexity constraints.

11. The computer automated placement method of claim 7, wherein placing the plurality of components is done in a two-dimensional manner with a plurality of overlapping rows.

12. The computer automated placement method of claim 7, wherein analyzing the layout is performed by calculating an overall unidirectional current density for the layout.

13. A computerized method of placing a plurality of components of an integrated circuit in a layout, the method comprising:

assigning each one of a plurality of components of an integrated circuit to one of a plurality of clusters;

generating a layout for each one of the plurality of clusters;

placing each one of the plurality of clusters in a layout for the integrated circuit wherein the placing is performed in a two-dimensional manner with a plurality of overlapping rows;

analyzing the layout for the integrated circuit using a cost function having a reliability verification factor; and

rearranging the layout for the integrated circuit; and

repeating the analyzing and the rearranging until the cost function is minimized.

14. The computerized method of claim 13, wherein the reliability verification factor represents the effects of electromigration and self heat.

15. The computerized method of claim 13, wherein a width of each one of the plurality of overlapping rows is a multiple of a smallest one of the plurality of clusters.

16. The computerized method of claim 14, wherein assigning each one of the components is performed based on a lumped gate ordering style.

17. The computerized method of claim 14, wherein assigning each one of the components is performed based on a distributed gate ordering style.

18. The computerized method of claim 14, further comprising adjusting one or more of the plurality of components in one of the clusters to comply with a size constraint.

19. The computerized method of claim 18, wherein the adjusting is performed using device-based legging.

20. The computerized method of claim 18, wherein the adjusting is performed using stack-based legging.

21. The computerized method of claim 18, wherein the adjusting is performed using differential legging.

22. An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

receive a circuit design;

receive at least one layout rule based on a reliability verification constraint for the circuit design; and

generate a layout for the circuit design through computer automated operations wherein the layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

23. The article of claim 22, wherein the reliability verification constraint arises from electromigration.

24. The article of claim 22, wherein the reliability verification constraint arises from self-heat.

25. The article of claim 22, wherein the layout is generated in a two dimensional manner having a plurality of overlapping rows.

26. An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

place a plurality of components of an integrated circuit design in a two-dimensional layout for the integrated circuit design;

analyze the layout for reliability verification considerations; and

rearrange the components to improve the reliability verification considerations based on the analysis of the layout.

27. The article of claim 26, wherein the reliability verification consideration arises from electromigration.

28. The article of claim 26, wherein the reliability verification consideration arises from self-heat.

29. A computer-readable medium having computer-executable modules comprising:

a cell library to maintain a plurality of logic gates and a plurality of layout rules;

a schematic design tool to create a schematic of an integrated circuit using the plurality of gates maintained by the cell library;

a net list tool to create a net list representation of the schematic; and

a placement tool to generate a layout of the integrated circuit from the net list representation wherein the placement tool performs a reliability verification of the layout.

30. The computer-readable medium of claim 29 further comprising a routing tool to route wires between the plurality of logic gates in the layout.

31. A computerized system comprising:

a computer-readable medium;

a processor; and

a computer-aided design program stored on the computer-readable medium and executable by the processor, the computer-aided design program comprising a

placement module to generate a layout of an intregrated circuit wherein the placement module performs a reliability verification of the layout.